WHAT IS CLAIMED IS:

1. A device comprising:

electrode means comprising at least one electrode for controlling a light modulating element of an array of light modulating elements; and

recursive feedback control means for controlling at least one pulse width using recursive feedback, said pulse width driving said electrode means.

2. The device of claim 1, wherein said recursive feedback is based on an output bit.

3. The device of claim 1, wherein said output bit is a drive output bit.

4. The device of claim 1, wherein said output bit is an intermediate output bit.

5. The device of claim 1, wherein said device includes a backplane and wherein said backplane includes said recursive feedback control means.

6. The device of claim 1, wherein said device includes a panel interface controller and wherein said panel interface controller includes said recursive feedback control means.

7. The device of claim 1, wherein said electrode means comprises at least two electrodes.

8. The device of claim 1, wherein said array of light modulating elements is part of a visual display apparatus.

9. The device of claim 1, wherein said array of light modulating elements on a single silicon backplane.

10. The device of claim 1, wherein said recursive feedback is explicit.

11. The device of claim 1, wherein said recursive feedback is implicit.

12. The device of claim 1, wherein said at least one pulse width comprises at least two pulse widths.

13. The device of claim 1, wherein said device include a plurality of pixel value bits for controlling a pixel value of said pulse width and wherein said recursive feedback control means only uses some of said pixel value bits to determine a next state of said pulse width.

14. The device of claim 1, further comprising a visual display apparatus including said array of light modulating elements.

15. The device of claim 14, wherein said visual display apparatus is an LCoS device and wherein said visual display apparatus includes pH indicating means indicating when a liquid crystal and/or the environment surrounding said liquid crystal of said visual display apparatus is damaged.

16. A method comprising the following steps:

(a) controlling at least one pulse width using recursive feedback; and

(b) driving an electrode means using said pulse width to thereby control a light modulating element of an array of light modulating elements.

17. The method of claim 16, wherein step (a) comprise a series of stages each having a stage value, wherein a plurality of bit locations are associated with a pixel value of said light modulating element, wherein at any given stage of said series of stages a subset of said bit locations are required to determine a next state of said light modulating element, and wherein said subset is determined based on said stage value.

18. The method of claim 17, wherein at a given stage only zeros in said stage value are required to determine said subset of said bit locations.

19. The method of claim 17, wherein at a given stage only ones in said stage value are required to determine said subset of said bit locations.

20. The method of claim 17, wherein said method further comprises the following step:

(c) logically combining said subset of said bit locations to form a logical combination, wherein said recursive feedback comprises combining said logical combination with a current output bit to determine a next output bit, and wherein in step (b) said next output bit is used to drive said electrode means.

21. The method of claim 20, wherein said recursive feedback is explicit.

22. The method of claim 20, wherein said recursive feedback is implicit.

23. The method of claim 20, wherein at least some bit locations of said subset of said bit locations are held on a single substrate.

24. The method of claim 23, wherein all of said bit locations of said subset of bit locations are held on said single substrate.

25. The method of claim 23, wherein said substrate comprises a semiconductor material.

26. The method of claim 25, wherein said substrate comprises silicon.

27. The method of claim 17, wherein said next state of said modulating output is based on a sticky logical OR or a sticky logical AND of said subset of said bit locations.

28. The method of claim 16, wherein said light modulating elements are part of a visual display apparatus.

29. The method of claim 16, wherein said method is implemented in a computer system.

30. A system comprising:

means for controlling at least one pulse width using recursive feedback; and

means for driving an electrode means using said pulse width to thereby control a light modulating element of an array of light modulating elements.

31. A device comprising:

an array of storage bits for controlling an array of outputs; and

updating means for conditionally updating said storage bits.

32. The device of claim 31, wherein said device comprises a light modulating device.

33. The device of claim 31, wherein said updating means includes means for performing a mask write operation.

34. The device of claim 33, wherein said mask write operation supports the setting or resetting of one of said storage bits.

35. The device of claim 31, wherein each of said storage bits is capable of being set or reset.

36. The device of claim 31, wherein said array of outputs control light modulating elements.

37. The device of claim 36, wherein said device further comprises a visual display apparatus comprising said light modulating elements.

38. The device of claim 37, wherein said visual display apparatus is an LCoS device and wherein said visual display apparatus includes pH indicating means indicating when a liquid crystal and/or the environment surrounding said liquid crystal of said visual display apparatus is damaged.

39. A method comprising:

forming a plurality of single pulses by performing two series of count steps for each of said plurality of single pulses, and

controlling an array of light modulating elements using a respective single pulse of said plurality of single pulses for each light modulating element of said array.

40. The method of claim 39, wherein either of said two series of count steps of is controlled by a recursive feedback process.

41. The method of claim 39, wherein one of said two series of count steps controls where said single pulse starts and the other said two series of count steps controls when said single pulse ends.

42. The method of claim 39, wherein said two series of count steps comprises: a series of LS count steps and a series of MS count steps.

43. The method of claim 39, wherein said count steps conditionally set or clear an output bit based on a set of pixel values for said array of light modulating elements.

44. The method of claim 43, wherein said pixel values are stored in storage bits and any of said storage bits that are not used for controlling a pulse width of one or more selected single pulses of said plurality of single pulses may be reallocated for storing values unrelated to said one or more selected single pulses.

45. The method of claim 44, wherein all of said storage bits that control all of said pulse widths are less than the sum total of the number of bits that control the pulse width multiplied by the number of light modulating elements.

46. The method of claim 39, wherein further said light modulating elements are part of a visual display apparatus.

47. A system comprising:

means for forming a plurality of single pulses by performing two series of count steps for each of said plurality of single pulses, and

means for controlling an array of light modulating elements using a respective single pulse of said plurality of single pulses for each light modulating element of said array.

48. A device comprising:

an array of light modulating elements; and

means for generating pulse widths for each of said light modulating elements using bit serial processing.

49. The device of claim 48, wherein said bit serial processing requires only logical bit serial operations.

50. The device of claim 48, wherein said bit serial processing uses logical and/or arithmetic bit serial operations.

51. The device of claim 48, wherein said light modulating elements are part of a visual display apparatus.

52. The device of claim 48, wherein said light modulating elements are arranged in a two-dimensional array.

53. The device of claim 52, wherein said device includes two arrays of processing elements and wherein said two arrays of processing elements are located on opposite sides of said array of light modulating elements.

54. The device of claim 48, wherein said device further comprises: at least one array of processing elements for computing pulse widths that control said light modulating elements.

55. The device of claim 54, wherein said array of light modulating elements comprises a first group of light modulating elements and a second group of light modulating elements, and wherein said at least one array of processing elements comprises a first array of processing elements and a second array of processing elements for controlling, respectively, said first group of light modulating elements and said second group of light modulating elements independently of each other.

56. The device of claim 55, wherein said array of light modulating elements is comprised of two partial arrays, and wherein said first group of light modulating elements and said second group of light modulating elements include each include light modulating elements in each of said two partial arrays.

57. The device of claim 56, further comprising a set of one or more first arrays of storage bits and a set of one or more second arrays of storage bits, wherein said first array of processing elements reads and processes data from said set of one or more first arrays of

storage bits and wherein said second processing element reads and processes data from said set of one or more second arrays of storage bits.

58. The device of claim 48, further comprising a visual display apparatus including said light modulating elements.

59. The device of claim 58, wherein said visual display apparatus is an LCoS device and wherein said visual display apparatus includes pH indicating means indicating when a liquid crystal and/or the environment surrounding said liquid crystal of said visual display apparatus is damaged.

60. A method comprising:

providing an array of light modulating elements; and

generating pulse widths for each of said light modulating elements using bit serial processing.

61. The method of claim of claim 60, wherein said bit serial processing uses only logical bit serial operations.

62. The method of claim 60, wherein said bit serial processing uses logical and/or arithmetic bit serial operations.

63. The method of claim 60, wherein said light modulating elements are part of a visual display apparatus.

64. A system comprising:

an array of light modulating elements; and

means for generating pulse widths for each of said light modulating elements using bit serial processing.

65. A device comprising:

a substrate;

an array of electrodes for controlling light modulating elements, said electrodes being located on said substrate; and

an array of bit serial processing elements for controlling said light modulating elements, said bit processing elements being located on said substrate.

66. The device of claim 65, further comprising a visual display apparatus including said light modulating elements.

67. The device of claim 66, wherein said visual display apparatus is an LCoS device and wherein said visual display apparatus includes pH indicating means indicating when a liquid crystal and/or the environment surrounding said liquid crystal of said visual display apparatus is damaged.

68. A device comprising:

a two-dimensional array of light modulating elements;

output bits for controlling each of said light modulating elements;

reading means for reading one bit position of pixel values for a one-dimensional array of light modulating elements of said two-dimensional array of light modulating elements; and

means for computing a one-dimensional array of control signals for said output bits based on one or more sets one-bit positions of said pixel values, wherein said control signals are capable of being used to control a next value of each of said output bits to thereby control each of said light modulating elements.

69. The device of claim 68, wherein said control signals control the setting or resetting of each of said output bits.

70. The device of claim 68, wherein each of said output bits is based on said control signals.

71. The device of claim 68, further comprising pixel value control means for controlling addressing of said one bit position of pixel values.

72. The device of claim 68, further comprising output bit control means for controlling addressing of each of said output bits.

73. The device of claim 68, further comprising computing control means for controlling said computing means.

74. The device of claim 68, further comprising a visual display apparatus including said light modulating elements.

75. The device of claim 74, wherein said visual display apparatus is an LCoS device and wherein said visual display apparatus includes pH indicating means indicating when a liquid crystal and/or the environment surrounding said liquid crystal of said visual display apparatus is damaged.

76. A method comprising the following steps:

(a) inputting partially or fully encoded pixel values for an array of light modulating elements using digital processing to convert said pixel values to pulse widths; and

(b) controlling a plurality of light modulating elements of said array of light modulating elements using a series of instructions to control multiple data path elements.

77. The method of claim 76, wherein step (a) is performed in a series of stages.

78. The method of claim 77, wherein each stage is controlled by said series of instructions.

79. The method of claim 78, wherein there are a different number of instructions for at least some of said stages.

80. The method of claim 77, wherein a different subset of bits of said pixel values are used to determine an output control for each stage.

81. The method of claim 76, wherein step (a) comprises using recursive feedback digital processing.

82. The method of claim 76, wherein step (a) comprising using bit serial digital processing.

83. The method of claim 76, wherein results from said digital processing are save in a buffer prior to step (b).

84. The method of claim 76, wherein said method is implemented in a computer system.

85. A system comprising:

means inputting partially or fully encoded pixel values for an array of light modulating elements using digital processing to convert said pixel values to pulse widths; and

means for controlling a plurality of light modulating elements of said array of light modulating elements using a series of instructions to control multiple data path elements.

86. A method comprising:

controlling at least one pulse width using a recursive feedback process; and

controlling an array of electrodes using said at least one pulse width, wherein said recursive feedback process is performed using bit serial processing.

87. The method of claim 86, wherein said array of electrodes is a two-dimensional array.

88. The method of claim 87, wherein said bit serial processing is performed by one or more one-dimensional arrays of bit serial processing elements.

89. A system comprising:

means controlling at least one pulse width using a recursive feedback process; and

means for controlling an array of electrodes using said at least one pulse width, wherein said recursive feedback process is performed using bit serial processing.

90. A method comprising the following steps:

(a) providing available memory on a spatial light modulator; and

(b) reallocating said available memory for data on said spatial light modulator, wherein space allocated is based on the length of time that said data needs to stay resident on said spatial light modulator and wherein said data is processed to control electrodes on said spatial light modulator.

91. The method of claim 90, wherein said data are a bit position array that partially specifies at least one pulse width on said control electrodes.

92. The method of claim 91, wherein different bit positions of said plurality of bit positions require different amounts of said available memory.

93. The method of claim 92, wherein the amount of said available memory required for said bit positions is based on the amount of time that a selected bit position of a selected pixel of said plurality of pixels must stay resident on said spatial light modulator.

94. The method of claim 91, wherein buffer sizes for each of said plurality of bit positions is variable.

95. The method of claim 91, wherein the number of said bit positions is a variable number.

96. The method of claim 91, wherein said bit positions comprise a two-dimensional array of bit positions.

97. The method of claim 96, wherein one dimension of said array is based on the line width of said spatial light modulator.

98. The method of claim 90, wherein step (b) employs a non-circular buffer.

99. The method of claim 90, wherein step (b) employs a circular buffer.

100. The method of 90, wherein said data is fetched from an external memory and sent on a backplane for said spatial light modulator in coordination with step (b).

101. A system comprising:

means for providing available memory on a spatial light modulator; and

means for reallocating said available memory for data on said spatial light modulator, wherein space allocated is based on the length of time that said data needs to stay resident on

said spatial light modulator and wherein said data is processed to control electrodes on said spatial light modulator.

102. A device comprising:

a backplane comprising an instruction memory for holding instructions for controlling at least one pulse width on each light modulating element of a spatial light modulator.

103. The device of claim 102, wherein said backplane further comprises a RAM for said instruction memory.

104. The device of claim 103, wherein said instruction memory is ROM.

105. The device of claim 102, wherein said instructions are for controlling memory pointers for reading a plurality of bit positions that control each of said light modulating elements.

106. The device of claim 105, wherein said memory pointers move in a circular buffer fashion.

107. The device of claim 105, wherein changing initial contents of said memory pointers modifies the timing and/or number of pulse widths driving each of said light modulating elements.

108. The device of claim 105, wherein said backplane further comprises a pointer memory array and said memory pointers are held in said pointer memory array.

109. The device of claim 105, wherein at least some of said memory pointers point to the same bit position of said plurality of bit positions.

110. The device of claim 109, wherein said instruction memory includes said pointer memory array.

111. The device of claim 102, wherein said backplane further comprises memory pointers, wherein at least some of said memory pointers are modified by a common set of logic controlled by said instructions.

112. The device of claim 102, wherein said instruction memory holds a sequence of operations comprising said instructions, wherein said sequence of operations repeats at a periodic rate.

113. The device of claim 112, wherein said periodic rate is based on a line rate of a display process of said spatial light modulator.

114. The device of claim 102, wherein changing said instructions modifies the timing and/or number of pulse widths driving each of said light modulating elements.

115. The device of claim 102, wherein changing said instructions modifies the number of bit positions per pixel value.

116. The device of claim 102, further comprising means for reloading said instruction memory while said device continues to control said spatial light modulator.

117. The device of claim 102, wherein said holding instructions control one or more array of processing elements.

118. The device of claim 117, further comprising said processing elements.

119. The device of claim 102, wherein said instructions control pointers to a MRAM memory array.

120. A device comprising:

a backplane for a spatial modulator;

a plurality of pointers to bit position array on said backplane; and

pointer controller means for controlling said plurality of pointers.

121. The device of claim 120, wherein said pointer controller means is located on said backplane.

122. The device of claim 120, wherein said pointer controller means is external on said backplane.

123. The device of claim 120, wherein a portion of said pointer controller means is on said backplane and a portion of said pointer controller means is external on said backplane.

124. The device of claim 120, wherein said pointer controller means comprises a sequencing means for manipulating said pointers in sequence.

125. The device of claim 120, wherein said pointer controller means controls at least one circular buffer on said backplane.

126. A method comprising:

storing a first group of bit positions of a plurality of pixels in bit position arrays on a backplane, said first group of bit positions comprising a contiguous group of bit positions;

storing at least one second group of bit positions on said backplane, said second group of bit positions corresponding to a subset of said plurality of pixels; and

combining on said backplane said first group and said at least one second group to thereby control a pulse width of one or more light modulating elements, wherein said second group of bit positions is stored for a shorter period of time on said backplane than said first group of bit positions is stored on said backplane.

127. A system comprising:

means for storing a first group of bit positions of a plurality of pixels in bit position arrays on a backplane, said first group of bit positions comprising a contiguous group of bit positions;

means for storing at least one second group of bit positions on said backplane, said second group of bit positions corresponding to a subset of said plurality of pixels; and

means for combining on said backplane said first group and said at least one second group to thereby control a pulse width of one or more light modulating elements, wherein

said second group of bit positions is stored for a shorter period of time on said backplane than said first group of bit positions is stored on said backplane.

128. A method comprising:

storing a first group of bit positions of a plurality of pixels in bit position arrays on a backplane, said first group of bit positions comprising a contiguous group of bit positions;

storing at least one summary bit of said plurality of pixel value on said backplane, and

combining on said backplane said first group and said at least one summary bit to thereby control a pulse width of one or more light modulating elements, wherein said summary bit is stored for a shorter period of time on said backplane than said first group of bit positions is stored on said backplane.

129. The method of claim 128, wherein said summary bit is based on selected bit positions and said selected bit positions are selected based on a count step for controlling said pulse width.

130. A system comprising:

means for storing a first group of bit positions of a plurality of pixels in bit position arrays on a backplane, said first group of bit positions comprising a contiguous group of bit positions;

means for storing at least one summary bit of said plurality of pixel value on said backplane, and

means for combining on said backplane said first group and said at least one summary bit to thereby control a pulse width of one or more light modulating elements, wherein said summary bit is stored for a shorter period of time on said backplane than said first group of bit positions is stored on said backplane.

131. A device comprising:

an array of circuits comprising:

means for voltage level shifting;

a selectable logic function based on a memory bit; and

means for controlling one or more light modulating elements, wherein a constant voltage source is used for said array of circuits.

132. The device of claim 131, wherein said means for voltage level is capable of outputting a voltage higher than a voltage on said memory bit.

133. The device of claim 131, wherein said selectable logic function selects whether a bit is inverted or not.

134. The device of claim 131, wherein said selectable logic function forces an output of said array of circuits high or low.

135. The device of claim 131, wherein said device uses at least 2 cross-coupled P-channel transistors to pull up said array of circuits to a logic that one P-channel transistor is off when the other P-channel transistor is on.

136. The device of claim 135, further comprising a plurality of N-channel transistors connected to each of said P-channel transistors for pulling down no more than one of said P-channel transistors at one time.

137. The device of claim 135, further comprising a plurality of nodes that are either driven to low or allowed to float, wherein when one of said nodes is driven to ground thereby causing one of said P-channel transistors to be pulled to ground thus turning on a gate of said other P-channel transistor.

138. The device of claim 137, wherein corresponding nodes of said plurality of nodes of a subset of said array of circuits are electrically connected.

139. The device of claim 138, wherein a sequence of writing values to said memory bit and sensing one or more of said corresponding nodes include means for testing the functionality of said means for voltage level shifting and/or said memory bit.

140. The device of claim 131, wherein said array of circuits is an inherently testable array of circuits.

141. The device of claim 140, wherein said nodes must be sensed in order to test said array of circuits.

142. A method comprising:

determining a pulse wave form for each line of a two-dimensional array of drive bits using a recursive feedback process, wherein each drive bit in said array of drive bits is in an initialized state; and

turning all of said drive bits to an off state to thereby produce a blanking interval between fields for an image, wherein control of each of said pulse wave forms is staggered in time.

143. A system comprising:

means for determining a pulse wave form for each line of a two-dimensional array of drive bits using a recursive feedback process, wherein each drive bit in said array of drive bits is in an initialized state; and

means for turning all of said drive bits to an off state to thereby produce a blanking interval between fields for an image, wherein control of each of said pulse wave forms is staggered in time.

144. A device comprising:

a spatial light modulator comprising an array of master-slave bit pairs, wherein for each master-slave bit pair a master bit includes means for selectively driving a corresponding slave bit, and wherein both said master bit and said corresponding slave bit are capable of being randomly accessed.

145. The device of claim 144, wherein said slave bit is a bit of a MRAM array.

146. The device of claim 144, wherein said MRAM array includes means for supporting a masked write operation.

147. The device of claim 144, wherein said spatial light modulator further comprises means for initiating a transfer from each master to a respective slave bit at substantially the same time.

148. A method comprising:

providing an m bit input pixel value; and

mapping said m bit input pixel value into a non-binary weighted single pulse using time based remapping to thereby control a light modulating element of a spatial light modulator.

149. The method of claim 148, wherein said single pulse is controlled by a single count process.

150. The method of claim 148, wherein said single pulse is controlled by a dual count process.

151. The method of claim 148, said single pulse performs gamma correction of light output of said spatial light modulator.

152. A system comprising:

means for providing an m bit input pixel value; and

means for mapping said m bit input pixel value into a non-binary weighted single pulse using time based remapping to thereby control a light modulating element of a spatial light modulator.

153. A device comprising:

a backplane controller including means for sequencing a series of instructions, wherein said instructions control memory accesses to data that is used to control one or more pulse widths on a spatial light modulator.

154. The device of claim 153, wherein device further includes memory in which said instructions are stored.

155. The device of claim 154, wherein said memory is RAM.

156. The device of claim 153, wherein said instructions control which of said data is accessed.

157. The device of claim 153, wherein said instructions control which drive bits of said spatial light modulator are enabled to be modified.

158. A method comprising:

mapping an input pixel value for each pixel of an array of pixels to a first output pixel value using a first time base to generate first pulse width; and

mapping said input pixel value to a second output pixel value using a second time base to generate a second pulse width to thereby reduce the worse case phase difference in adjacent pixels of a spatial light modulator, wherein said adjacent pixels of said array of pixels have respective input pixel values that differ by 1 LS-bit.

159. The method of claim 158, wherein said worse case phase difference between said adjacent pixels only occurs in one of two fields of an image formed by said array of pixels.

160. A system comprising:

means for mapping an input pixel value for each pixel of an array of pixels to a first output pixel value using a first time base to generate first pulse width; and

means for mapping said input pixel value to a second output pixel value using a second time base to generate a second pulse width to thereby reduce the worse case phase difference in adjacent pixels of a spatial light modulator, wherein said adjacent pixels of said array of pixels have respective input pixel values that differ by 1 LS-bit.

161. A device comprising:

a MRAM array of MRAM storage bits for a spatial light modulator, said MRAM storage bits being arranged in MRAM columns; and

bit lines for each of said MRAM columns, wherein said bit lines support a first and a second driver on opposite sides of said array, wherein said MRAM storage bits are for a spatial light modulator.

162. The device of claim 161, further comprising said first driver and said second driver.

163. The device of claim 162, wherein said first driver and said second driver each include means for masked writing to said MRAM storage bits.

164. The device of claim 161, further comprising a first processing means and a second processing means for writing to said MRAM storage bits, wherein said first processing means and said second processing means are located on opposite sides of said MRAM array and wherein either said first processing means or said second processing means is capable of writing to said MRAM storage bits on either side of said MRAM array.

165. The device of claim 161, further comprising ERAM storage bits interposed between said MRAM storage bits of said MRAM array.

166. The device of claim 165, wherein said ERAM storage bits is arranged in ERAM columns, wherein said ERAM columns form two separate ERAM memory arrays, and wherein each of said ERAM memory arrays includes inputs and outputs on opposite sides thereof.

167. A device comprising:

an array of drive bits; and

means for performing a masked write to said drive bits.

168. The device of claim 167, wherein said drive bits are part of a spatial light modulator.